MEASUREMENT OF PACKAGE INTERCONNECT IMPEDANCE USING TESTER AND SUPPORTING TESTER HARDWARE

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Related Application (Priority Claim)

This application is a continuation-in-part of U.S. patent application Serial No. 10/448,987, filed May 30, 2003.

Background

The present invention generally relates to methods and apparatuses for measuring package interconnect impedance, and more specifically relates to a method and apparatus for measuring the impedance of a substrate trace in a consistent manner for large sample sizes, multiple traces, in an automated fashion.

Presently, there is no widely available method and apparatus for monitoring impedance tolerance across different substrate families with various process/assembly variations. There is no widely available method and apparatus that can measure any trace on a package, can measure multiple traces at high speed, in an automated matter. There is no widely available method and apparatus which standardizes the impedance measurement technique and which can be implemented at necessary sites.

Objects and Summary

An object of an embodiment of the present invention is to provide a method and apparatus which can monitor impedance tolerance across different substrate families with various process/assembly variations.

Another object of an embodiment of the present invention is to provide a method and apparatus which can measure any trace on a package, and which can measure multiple traces at high speed, in an automated matter.

Yet another object of an embodiment of the present invention is to provide a method and apparatus which can standardize the impedance measurement technique and which can be implemented at necessary sites.

Briefly, and in accordance with at least one of the foregoing objects, an embodiment of the present invention provides a method and apparatus wherein a test head from a tester is used to mount a probe card. A device under test (DUT)/load board is provided, and the DUT/load board has a socket which is configured to hold a substrate. Probe pins from the probe card make contact with bump pads on the substrate. The probe card is either fully populated to meet the bump pads on the substrate, and all except one pin are grounded. Signal wires from the DUT/load board are fed to the tester, and the tester is connected to a Digital Sampling Oscilloscope (DSO) with a fast rise time signal head. During testing, a signal is launched using the DSO into a coaxial cable which is connected to the probe card via the test head. The launched signal and the reflected signal are captured back by the DSO, and then fed into the tester via GPIB connections (i.e., a GPIB cable). Using this data, post processing software is used to obtain the

interconnect impedance versus time for the device (i.e., package) under test. The method and apparatus can be used in connection with both Flip Chip and Wire bonded products.

In another embodiment, the final test socket mounted on the load board is used. Specifically, the substrate with solder balls attached is dropped into the socket, and the DSO is connected to the tester head with a GPIB cable and to the DUT/load board with a coaxial cable. The DUT/load board, already attached to the tester head, can then be used to measure the impedance.

Brief Description of the Drawings

The organization and manner of the structure and operation of the invention, together with further objects and advantages thereof, may best be understood by reference to the following description, taken in connection with the accompanying drawing, wherein:

FIGURE 1 illustrates an apparatus which is in accordance with an embodiment of the present invention;

FIGURE 2 provides a block diagram which illustrates a method which is in accordance with an embodiment of the present invention;

FIGURE 3 illustrates an apparatus which is in accordance with an alternative embodiment of the present invention;

FIGURE 4 is similar to FIGURE 3, but provides a cross-sectional view.

Description

While the invention may be susceptible to embodiment in different forms, there are shown in the drawings, and herein will be described in detail, specific embodiments with the understanding that the present disclosure is to be considered an exemplification of the principles of the invention, and is not intended to limit the invention to that as illustrated and described herein.

As shown in the FIGURES 1 and 2, an embodiment of the present invention provides a method and apparatus wherein a tester head 10 of a tester 12 is used to mount a probe card 14. A device under test (DUT)/load board 16 is provided, and the DUT/load board 16 has a socket 18 which is configured to hold a substrate 20 having solder balls 21. Probe pins 22 from the probe card 14 make contact with bump pads 24 on the substrate 20. The probe card 14 is fully populated to meet the bump pads 24 on the substrate 20, and all except one pin are grounded. The tester 12 is connected to a Digital Sampling Oscilloscope (DSO) 28 with a fast rise time signal head. During testing, a signal is launched using the DSO into a coaxial cable 30 which then connects to the tester head 10. The launched signal and the reflected signal are captured back by the DSO 28, and then fed into the tester 12 via GPIB connections (i.e., a GPIB cable 32). Using this data, post processing software 34 is used to obtain the interconnect impedance versus time for the device (i.e., package) under test. The method and apparatus can be used in connection with both Flip Chip and Wire bonded products.

Most preferably, the tester head 10 selects the pin that is going to be the signal in the probe card 14 and makes the rest of the pins ground. Then, the tester head 10 lets the TDR signal out the selected pin using the coaxial cable 30 and then allows the reflection

from the DUT to get back to the TDR scope 28. The tester head 10 then uses the GPIB cable 32 connected to the DSO 28 to obtain the wave form and stores the data in a file.

FIGURES 3 and 4 illustrate an alternative embodiment. As shown, the final test socket 40 mounted on the load board 16 is used. Specifically, the substrate 20 with solder balls 21 attached is dropped into the socket 40, and the DSO 28 is connected to the tester 12 with a GPIB cable 32 and to the tester head 10 with a coaxial cable 30. The tester head 10 selects the pin that is going to the signal in the socket 40 and makes the rest of the pins ground. Then, the tester head 10 lets the TDR signal out the selected pin using the coaxial cable 30 and then allows the reflection from the DUT to get back to the TDR scope 28. The tester head 10 then uses the GPIB cable 32 connected to the DSO 28 to obtain the waveform and stores the data in a file. Post processing software 34 is used to obtain the interconnect impedance versus time for the device (i.e., package) under test.

Both embodiments of the present invention can monitor impedance tolerance across different substrate families with various process/assembly variations, can measure any trace on a package, and can measure multiple traces at high speed, in an automated matter. Both embodiments of the present invention can also standardize the impedance measurement technique and be implemented at necessary sites.

While embodiments of the present invention are shown and described, it is envisioned that those skilled in the art may devise various modifications of the present invention without departing from the spirit and scope of the appended claims.